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EXAMINER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte EDGAR R. ZUNIGA-ORTIZ and
SREENIVASAN K. KODURI

Appeal 2009-011686
Application 10/769,699
Technology Center 2800

Before ALLEN R. MACDONALD, CARLA M. KRIVAK, and
BRADLEY W. BAUMEISTER, *Administrative Patent Judges*.

BAUMEISTER, *Administrative Patent Judge*.

DECISION ON APPEAL¹

¹ The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the “MAIL DATE” (paper delivery mode) or the “NOTIFICATION DATE” (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 27-32. Claims 27, 28, and 30-32 stand rejected under 35 U.S.C. § 102(e) as anticipated by Yamazaki (US 6,709,901 B1, issued Mar. 23, 2004). Claim 29 stands rejected under 35 U.S.C. § 103(a) as obvious over Yamazaki in view of Akram (US 6,617,687 B2, issued Sep. 9, 2003).

We reverse.

[Appellants' invention relates to a] semiconductor chip having a planar active surface including an integrated circuit; the circuit has metallization patterns including a plurality of contact pads. Each of these contact pads has an added conductive layer on the circuit metallization. This added layer has a conformal surface adjacent the chip and a planar outer surface, and this outer surface is suitable to form metallurgical bonds without melting. The chip contact pads may have a distribution such that an area portion of the active chip surface is available for attaching a thermally conductive plate; this plate has a thickness compatible with the thickness of the conductive pad layer.

(Abstr.).

Independent claim 31 states, in relevant part:

A method of fabricating a semiconductor assembly comprising the steps of:

. . . providing an added conductive region having at least one conductive layer on [a semiconductor chip contact pad];

providing a [sic: an] assembly board having at least one *planar*, metallurgically bondable terminal pad; . . . and

metallurgically bonding said added conductive region and said at least one terminal pad. . . .

(App. Br. 8; emphasis added).

The Examiner finds that Yamazaki's method of attaching stick driver 208 to first substrate 201/220,² as depicted in Figure 10(B), reads on independent claim 31. Specifically, the Examiner finds that (1) the claimed semiconductor chip contact pad corresponds to Yamazaki's first conductive layer 221; (2) the claimed "added conductive region having at least one conductive layer" corresponds to the combination of second conductive layer 223 and gold plating layer 230, with the gold plating layer 230 corresponding to the claimed "conductive layer;" and (3) the claimed assembly board "terminal pad" corresponds to Yamazaki's input-output terminal 225 (Ans. 8-9).

Appellants argue, *inter alia*, that Yamazaki does not disclose a terminal pad connected directly to the bond pad as required by the claimed procedure, but rather discloses the use of an interposed barrier layer 229 (App. Br. 5).

We find Appellants' argument to be persuasive. Claim 31 requires that the metallurgical bonding of a contact pad's conductive region to a terminal pad that is planar. Yamazaki discloses that the gold plating layer 230 (which the Examiner finds to correspond to the conductive layer) is pressure welded to barrier layer 229 (col. 11, ll. 5-14). But barrier layer 229 is not planar (*see* Fig. 10B). As such, barrier layer 229 cannot be reasonably interpreted as constituting a planar terminal pad, as claimed.

² The first substrate is labeled as 201 in Figure 9 (*see* col. 10, l. 26), but alternatively labeled as 220 in Figure 10 (*see* col. 10, l. 52).

For the foregoing reasons,³ Appellants have persuaded us of error in the Examiner's anticipation rejection of independent claim 31. Accordingly, we will not sustain the Examiner's rejection of that claim or of claims 27, 28, 30, and 32, which depend from claim 31.

With respect to the remaining, obviousness rejection of dependent claim 29, the Examiner did not rely on Akram to cure the deficiency of the anticipation rejection explained above.

DECISION

The Examiner's decision rejecting claims 27-32 is reversed.

REVERSED

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³ Appellants further argue in the Reply Brief that claim 31 recites "providing a semiconductor chip having a planar active surface including an integrated circuit," but Yamazaki nowhere states that substrate 220 may specifically be an integrated circuit (Reply Br. 1). This argument was not timely presented in the Appeal Brief. We therefore do not address the question of whether Yamazaki discloses that substrate 220 may be an active surface of an integrated circuit instead of a glass substrate for supporting semiconductor thin films. *See Ex Parte Bordin*, 93 USPQ2d 1473, (BPAI 2010) (informative) ("conclud[ing] that the regulations set out in 37 C.F.R. § 41, *Practice Before the Board of Patent Appeals and Interferences*, do not require the Board to consider such belated arguments").